

What is claimed is:

1. A method of clock division, the method comprising:
counting positive edges of an input clock signal to provide a positive edge
count;
5 counting negative edges of the input clock signal to provide a negative
edge count;
providing a set of reference values, wherein the set of reference values
comprises a set of positive edge reference values and a set of negative edge reference
values;
10 comparing the positive edge count with each value of the set of positive
edge reference values;
comparing the negative edge count with each value of the set of negative
edge reference values; and
providing a divided clock signal in response to the comparisons such that
15 the divided clock signal is related to the clock signal by an amount.
2. The method of Claim 1, wherein providing the set of reference values
comprises:
receiving a mul signal, wherein the mul signal has a mul value that
corresponds to an integer; and
20 selecting the set of reference values from a table based upon the mul
value.
3. The method as in Claim 1, further comprising reducing jitter in the divided
clock signal.
4. The method of Claim 1, further comprising:
25 receiving a mul signal, wherein the mul signal has a mul value that
corresponds to an integer; and

adjusting the set of reference values in response to a change in the mul value, wherein the set of reference values are associated with a particular mul value.

5. The method of Claim 4, wherein the set of reference values comprises:
a pair of high-to-low reference values, wherein the pair of high-to-low
5 reference values is associated with positive and negative edge counts that are preselected for a falling edge in the divided clock signal; and
a pair of low-to-high references values, wherein the pair of low-to-high
reference values is associated with positive and negative edge counts that are preselected for a rising edge in the divided clock signal.

- 10 6. The method of Claim 1, wherein the set of reference values comprises a first reference value, a second reference value, a third reference value, a fourth reference value, a fifth reference value, and a sixth reference value, and wherein providing the divided clock signal comprises:
adjusting the divided clock signal such that the divided clock signal
15 corresponds to a first logical level when a first condition is satisfied, wherein the first condition is satisfied when the positive edge count is equal to the first reference value and the negative edge count is equal to the second reference value;
adjusting the divided clock signal such that the divided clock signal
corresponds to a second logical level when a second condition is satisfied, wherein the
20 second condition is satisfied when the positive edge count is equal to the third reference value and the negative edge count is equal to the fourth reference value, and wherein the second logical level is an inverse of the first logical level; and
adjusting the divided clock signal such that the divided clock signal
corresponds to the first logical level when a third condition is satisfied, wherein the third
25 condition is satisfied when the positive edge count is equal to the fifth reference value and the negative edge count is equal to the sixth reference value.

a lookup block that is configured to provide a set of reference signals in response to a mul signal, wherein the mul signal has an associated mul value that corresponds to an integer; and

a decode logic block that is configured to compare the positive edge count with each value of the set of positive edge reference values, compare the negative edge count with each value of the set of negative edge reference values, and provide a divided clock signal in response to the comparisons such that the divided clock signal is related to the clock signal by an amount.

12. The system of Claim 11, further comprising a reset logic block, wherein
10 the reset logic block is configured to:
assert a reset signal in response to a change in the mul value;
deassert the reset signal at least one clock after the reset signal is applied;
assert a negative edge count enable signal in response to a falling edge of
the input clock signal when the reset signal is deasserted; and
15 assert a positive edge count enable signal in response to a rising edge of
the input clock signal when the negative edge count enable signal is asserted.

13. The system of Claim 11, further comprising a reset logic block wherein the reset logic block is configured to:

assert a reset signal in response to a change in the mul value;

deassert the reset signal at least one clock after the reset signal is applied;

assert a positive edge count enable signal in response to a rising edge of the input clock signal when the reset signal is deasserted; and

assert a negative edge count enable signal in response to a falling edge of the input clock signal when the positive edge count enable signal is asserted.

25 14. The system of Claim 13, wherein the first counter block is configured to reset the positive edge count value to zero and stop counting when the reset signal is

asserted, and further configured to resume counting when a positive edge of the input clock signal occurs after the positive edge count enable signal is asserted, and wherein the second counter block is configured to reset the negative edge count value to zero and stop counting when the reset signal is asserted, and further configured to resume counting
5 when a negative edge of the input clock signal occurs after the negative edge count enable signal is asserted.

15. The system of Claim 11, further comprising a jitter minimizing block comprising:

10 a first flip-flop that is configured to provide a first clock signal in response to the divided clock signal, wherein the first flip-flop is triggered on rising edges of the input clock signal;

a second flip-flop that is configured to provide a second clock signal in response to the divided clock signal, wherein the second flip-flop is triggered on falling edges of the input clock signal; and

15 a multiplexer that is configured to select the first clock signal as a jitter-minimized divided output clock signal when the input clock signal corresponds to a low logical level, and further configured to select the second clock signal as the jitter-minimized divided clock output signal when the input clock signal corresponds to a high logical level.

20 16. The system of Claim 11, wherein a first of the set of reference signals has an associated first reference value, a second of the set of reference signals has an associated second reference value, a third of the set of reference signals has an associated third reference value, a fourth of the set of reference signals has an associated fourth reference value, a fifth of the set of reference signals has an associated fifth reference
25 value, a sixth of the set of reference signals has an associated sixth reference value, and wherein the decode logic block is arranged to provide the divided clock signal by:

resetting the negative count to one when a negative edge of the input clock signal occurs after the negative count reaches the mul value.

19. A system for clock division, the system comprising:

5 a first means for counting that is configured to count positive edges of an input clock signal to provide a positive edge count;

a second means for counting that is configured to count negative edges of the input clock signal to provide a negative edge count;

10 a first means for providing that is configured to provide a set of reference values, wherein the set of reference values comprises a set of positive edge reference values and a set of negative edge reference values;

a first means for comparing that is configured to compare the positive edge count with each value of the set of positive edge reference values;

a second means for comparing that is configured to compare the negative edge count with each value of the set of negative edge reference values; and

15 a second means for providing that is configured to provide a divided clock signal in response to the comparisons such that the divided clock signal is related to the clock signal by an amount.

20 20. The system of Claim 19, wherein the means for providing is arranged to provide the set of reference signals in response to a mul signal, the mul signal has an associated mul value that corresponds to an integer, the set of reference values comprises a first reference value, a second reference value, a third reference value, a fourth reference value, a fifth reference value, and a sixth reference value, and wherein the second means for providing comprises:

25 a first means for adjusting that is configured to adjust the divided clock signal such that the divided clock signal corresponds to a first logical level when a first condition is satisfied, wherein the first condition is satisfied when the positive edge count

is equal to the first reference value and the negative edge count is equal to the second reference value;

a second means for adjusting that is configured to adjust the divided clock signal such that the divided clock signal corresponds to a second logical level when a second condition is satisfied, wherein the second condition is satisfied when the positive edge count is equal to the third reference value and the negative edge count is equal to the fourth reference value, and wherein the second logical level is an inverse of the first logical level;

a third means for adjusting that is configured to adjust the divided clock signal such that the divided clock signal corresponds to the first logical level when a third condition is satisfied, wherein the third condition is satisfied when the positive edge count is equal to the fifth reference value and the negative edge count is equal to the sixth reference value;

a fourth means for adjusting that is configured to adjust the divided clock signal such that the divided clock signal corresponds to the second logical level when a fourth condition is satisfied, wherein the fourth condition is satisfied when the positive edge count is equal to one and the negative edge count is equal to zero; and

a fifth means for adjusting that is configured to adjust the divided clock signal such that the divided clock signal corresponds to the second logical level when a fifth condition is satisfied, wherein the fifth condition is satisfied when the positive edge count is equal to one and the negative edge count has reached the mul value.